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BURR - BROWN®

DAC725

Dual 16-Bit DIGITAL-TO-ANALOG CONVERTER

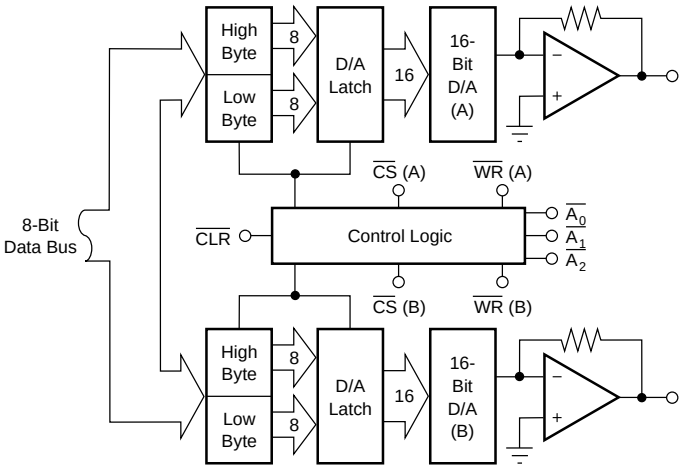
FEATURES

- **COMPLETE DUAL V_{OUT} DAC**
- **DOUBLE-BUFFERED INPUT REGISTER**
- **HIGH-SPEED DATA INPUT: Serial or Parallel**
- **HIGH ACCURACY: ±0.003% Linearity Error**
- **14-BIT MONOTONICITY OVER TEMPERATURE**
- **PLASTIC PACKAGE**
- **CLEAR INPUT TO SET ZERO OUTPUT**

DESCRIPTION

The DAC725 is a dual 16-bit DAC, complete with internal reference and output op amps. The DAC725 is designed to interface to an 8-bit microprocessor bus, but can also be interfaced to wider buses. The hybrid construction minimizes the digital feedthrough typically associated with products that combine the digital bus interface circuitry with high-accuracy analog circuitry.

The 16-bit data word is loaded into either of the DACs in two 8-bit bytes per 16-bit word. The versatility of the control lines allows the data word to be directed to either DAC, in any order. The voltage-out DACs are dedicated to a bipolar output voltage of ±10V. The output is immediately set to 0V when the Clear command is given. This feature, combined with the bus interfacing and complete DAC circuitry, makes the DAC725 ideal for automatic test equipment, power control, servo systems, and robotics applications.



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SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, V_{CC} = ±15V, and after a 10-minute warm-up unless otherwise noted.

PARAMETER	DAC725JP MIN	DAC725JP TYP	DAC725JP MAX	DAC725KP MIN	DAC725KP TYP	DAC725KP MAX	UNITS
INPUT							
DIGITAL INPUT							
Resolution			16			*	Bits
Bipolar Input Code		Binary Twos Complement			*		
Logic Levels[1]: V_{IH}	+2		+5.5	*		*	V
V_{IL}	–1		+0.8	*		*	V
I_{IH} (V_I = +2.7V)			1			*	µA
I_{IL} (V_I = +0.4V)			1			*	µA
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error		±0.003	±0.006		±0.0015	±0.003	% of FSR[2]
Differential Linearity Error[3]		±0.0045	±0.012		0.003	±0.006	% of FSR
At Bipolar Zero: KP[3, 4]					±0.003	±0.006	% of FSR
Gain Error[5]		±0.07	±0.2		*	±0.15	%
Bipolar Zero Error[5]		±0.05	±0.1		*	*	% of FSR
Montonicity Over Specified Temp. Range	13			14			Bits
Power Supply Sensitivity: $+V_{CC}$, $-V_{CC}$		±0.0015	±0.006		*	*	% of FSR/%V_{CC}
V_{DD}		±0.0001	±0.001		*	*	% of FSR/%V_{DD}
DRIFT (Over Specified Temperature Range)							
Gain Drift		±10			*	±25	ppm/°C
Bipolar Zero Drift		±5			*	±12	ppm of FSR/°C
Differential Linearity Over Temperature[3]		±0.0045	±0.012		±0.003	±0.006	% of FSR
Linearity Error Over Temperature[3]			±0.012			±0.006	% of FSR
SETTLING TIME (to ±0.003% of FSR)[6]							
20V Step (2kΩ load)		4			*	8	µs
1LSB Step at Worst-Case Code[7]		2.5			*	4	µs
Slew Rate		10			*		V/µs
OUTPUT							
Output Voltage Range[8]	±10			*			V
Output Current	±5			*			mA
Output Impedance		0.15			*		Ω
Short Circuit to Common Duration		Indefinite			*		
POWER SUPPLY REQUIREMENTS							
Voltage: $+V_{CC}$	+11.4	+15	+16.5	*	*	*	V
$-V_{CC}$	–11.4	–15	–16.5	*	*	*	V
V_{DD}	+4.5	+5	+5.5	*	*	*	V
Current (No load, ±15V supplies): $+V_{CC}$		+29	+35		*	*	mA
$-V_{CC}$		–35	–40		*	*	mA
V_{DD}		+6	+10		*	*	mA
Power Dissipation (±15V supplies)		920	1175		*	*	mW
TEMPERATURE RANGE							
Specification	0		+70	*		*	°C
Storage	–60		+150	*		*	°C

*Specification same as model to the left.

NOTES: (1) Digital inputs are TTL, LSTTL, 54/74HC and 54/74HTC compatible over the specification temperature range. (2) FSR means Full-Scale Range. For example, for ±10V output, FSR = 20V. (3) ±0.0015% of FSR is equal to 1LSB in 16-bit resolution. ±0.003% of FSR is equal to 1LSB in 15-bit resolution. ±0.006% of FSR is equal to 1LSB in 14-bit resolution. (4) Error at input code 0000_H (BTC). (5) Adjustable to zero with external trim potentiometer. Adjusting the gain potentiometer rotates the transfer function around the bipolar zero point. (6) Maximum represents the 3σ limit. Not tested for this parameter. (7) The bipolar worst-case code change is $FFFF_H$ to 0000_H (BTC). (8) Minimum supply voltage for ±10V output swing is approximately ±13V. Output swing for ±12V supplies is at least ±9V.

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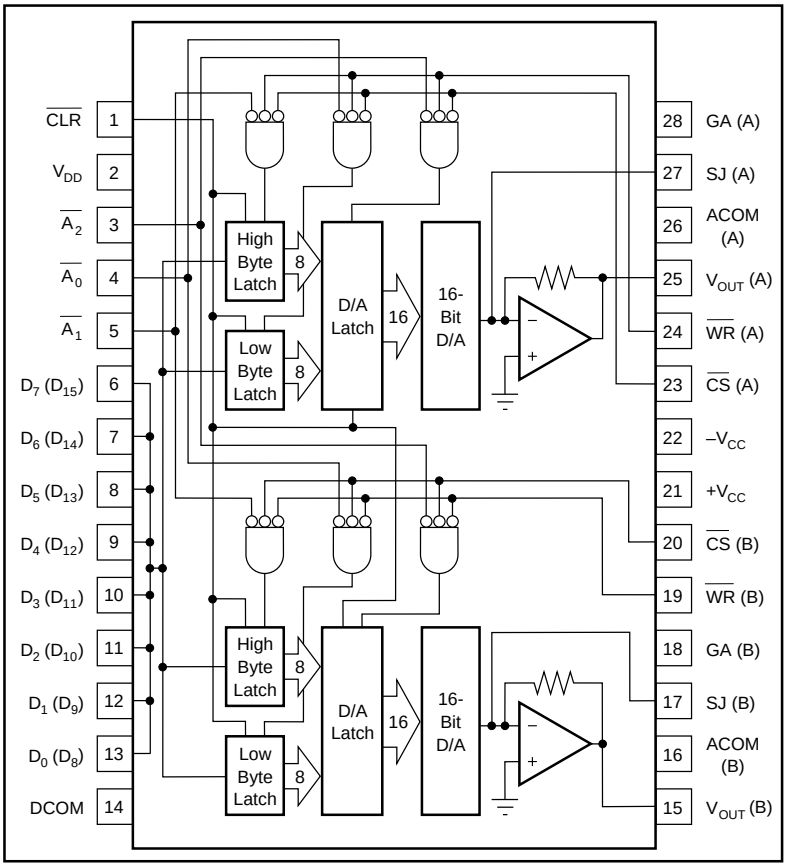
CONNECTION DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DD} to COMMON ..... 0V, +15V
$+V_{CC}$ to COMMON ..... 0V, +18V
$-V_{CC}$ to COMMON ..... 0V, –18V
Digital Data Inputs to COMMON ..... –0.5V, V_{DD} + 0.5
DC Current any Input ..... ±10mA
Reference Out to COMMON ..... Indefinite Short to COMMON
V_{OUT} ..... Indefinite Short to COMMON
External Voltage Applied to R_F ..... ±18V
External Voltage Applied to D/A Output ..... ±5V
Power Dissipation 2000mW
Storage Temperature ..... –60°C to +150°C
Lead Temperature (soldering, 10s) ..... 300°C

NOTE: These devices are sensitive to electrostatic discharge. Appropriate I.C. handling procedures should be followed.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ORDERING INFORMATION

MODEL	LINEARITY ERROR max (% of FSR)	TEMPERATURE RANGE
DAC725JP	±0.012	0°C to +70°C
DAC725KP	±0.006	0°C to +70°C

PIN DESCRIPTIONS

PIN	DESIGNATOR	DESCRIPTION
1	CLR	Clear line. Sets the D/A register to 0000_{HEX}, which gives bipolar zero on the D/A output.
2	V_{DD}	Logic supply (+5V).
3	$\overline{A_2}$	Latch enable for D/A latch (active low).
4	$\overline{A_0}$	Latch enable for "low byte" input (active low).
5	$\overline{A_1}$	Latch enable for "high byte" input (active low).
6	D_7 (D_{15}) (MSB)	Input for data bit 7 if enabling low byte (LB) latch, or data bit 15 if enabling the high byte (HB) latch.
7	D_6 (D_{14})	Input for data bit 6 if enabling LB latch, or data bit 14 if enabling HB latch.
8	D_5 (D_{13})	Data bit 5 (LB) or data bit 13 (HB).
9	D_4 (D_{12})	Data bit 4 (LB) or data bit 12 (HB).
10	D_3 (D_{11})	Data bit 3 (LB) or data bit 11 (HB).
11	D_2 (D_{10})	Data bit 2 (LB) or data bit 10 (HB).
12	D_1 (D_9)	Data bit 1 (LB) or data bit 9 (HB).
13	D_0 (D_8)	Data bit 0 (LB) or data bit 8 (HB).
14	DCOM	Digital common.
15	V_{OUT} (B)	Voltage output for DAC B.
16	ACOM (B)	Analog common for DAC B.
17	SJ (B)	Summing junction of the internal op amp for DAC B.
18	$\overline{GA}$ (B)	Gain adjust pin for DAC B.
19	$\overline{WR}$ (B)	Write control line for DAC B.
20	$\overline{CS}$ (B)	Chip select control line for DAC B.
21	$+V_{CC}$	Positive supply voltage (+15V).
22	$-V_{CC}$	Negative supply voltage (–15V).
23	$\overline{CS}$ (A)	Chip select control line for DAC A.
24	$\overline{WR}$ (A)	Write control line for DAC A.
25	V_{OUT} (A)	Voltage output for DAC A.
26	ACOM (A)	Analog common for DAC A.
27	SJ (A)	Summing junction of the internal op amp for DAC A.
28	GA (A)	Gain adjust pin for DAC A.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
DAC725JP	28-Pin Plastic DIP	215
DAC725KP	28-Pin Plastic DIP	215

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC725 accepts positive-true binary twos complement input code, as shown in Table I. The data is loaded into either DAC, 8 bits at a time. The data may also be clocked into the device in a serial format.

DIGITAL INPUT CODES	ANALOG OUTPUT (Binary Two's Complement, Bipolar Operation, All Models)
$7FFF_H$	+ Full Scale
0000_H	Zero
$FFFF_H$	– 1LSB
8000_H	– Full Scale

TABLE I. Digital Input Codes.

ACCURACY

Linearity

This specification describes one of the most important measures of performance of a D/A converter. Linearity error is the deviation of the analog output from a straight line drawn through the end points (minus full-scale point and plus full-scale point).

Differential Linearity Error

Differential Linearity Error (DLE) of a D/A converter is the deviation from an ideal 1LSB change in the output when the input changes from one adjacent code to the next. A differential linearity error specification of ±1/2LSB means that the output step size can be between 1/2LSB and 3/2LSB when the input changes between adjacent codes. A negative DLE specification of –1LSB maximum (–0.006% for 14-bit resolution) insures monotonicity.

Monotonicity

Monotonicity assures that the analog output will increase or remain the same for increasing input digital codes. The DAC725 is specified to be monotonic to 14 bits over the entire specification range.

DRIFT

Gain Drift

Gain drift is a measure of the change in full-scale range output over temperature expressed in parts per million per degree centigrade (ppm/°C). Gain drift is established by:

(1) testing the end point differences at t_{MIN}, +25°C and t_{MAX},

(2) calculating the gain error with respect to the +25°C value, and

(3) dividing by the temperature change.

The DAC725 is specified for Maximum Gain and Offset values at temperature. This tells the system designer the maximum that can be expected over temperature, regardless of room temperature values.

Zero Drift

Zero drift is a measure of change in the output with 0000_H applied to the D/A converter inputs over the specified temperature range. This code corresponds to 0V analog output.

The maximum change in offset at t_{MIN} or t_{MAX} is referenced to the zero error at +25°C and is divided by the temperature change. This drift is expressed in FSR/°C.

SETTLING TIME

Settling time of the D/A is the total time required for the analog output to settle within an error band around its final value after a change in digital input. Refer to Figure 1 for typical values for this family of products.

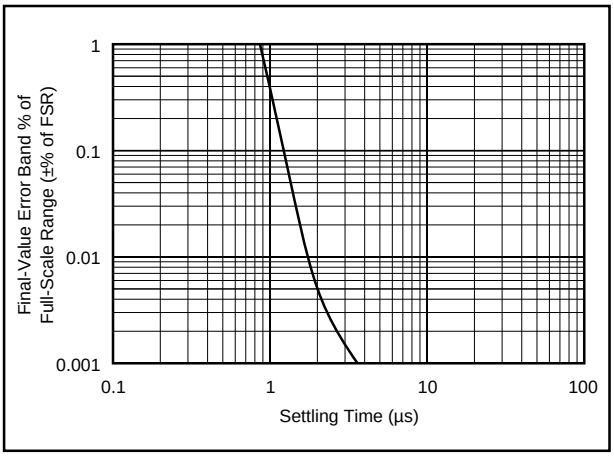


FIGURE 1. Final-Value Error Band Versus Full-Scale Range Settling Time.

Settling times are specified to ±0.003% of FSR (±1/2LSB for 14 bits) for two input conditions: a full-scale range change of 20V (±10V), and a 1LSB change at the "major carry," the point at which the worst-case settling time occurs. This is the worst-case point since all of the input bits change when going from one code to the next.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a change in a power supply voltage on the D/A converter output. It is defined as a percent of FSR change in the output per percent of change in either the positive supply ($+V_{CC}$), negative supply ($-V_{CC}$) or logic supply (V_{DD}) about the nominal power supply voltages (see Figure 2). It is specified for DC or low frequency changes. The typical performance curve in Figure 2 shows the effect of high frequency changes in power supply voltages.

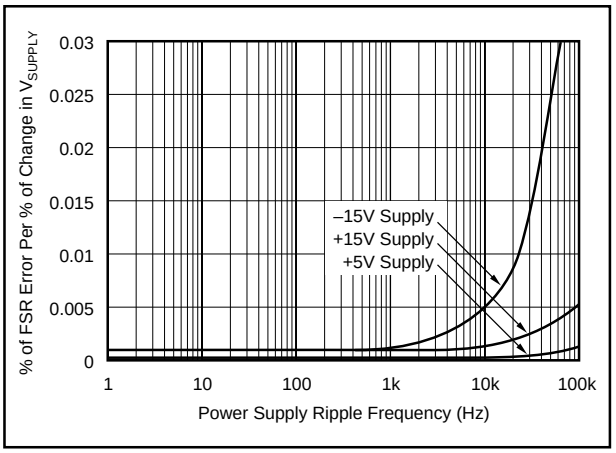


FIGURE 2. Power Supply Rejection Versus Power Supply Ripple Frequency.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. 1µF to 10µF tantalum capacitors should be located close to the D/A converter.

EXTERNAL ZERO AND GAIN ADJUSTMENT

Zero and gain may be trimmed by installing external zero and gain potentiometers. Connect these potentiometers as shown in the Connection Diagram and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 270kΩ resistors (±20% carbon or better) should be located close to the D/A converter to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 3, may be substituted in place of the 3.9MΩ resistor. A 0.001µF to 0.01µF low-leakage film capacitor should be connected from Gain Adjust to Analog Common to prevent noise pickup. Refer to Figure 4 for relationship of Offset and Gain adjustments.

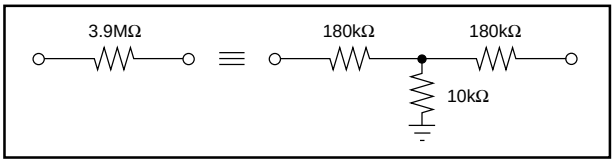


FIGURE 3. Equivalent Resistances.

Zero Adjustment

By loading the code 0000_H, the DAC will force 0V. Offset is adjusted by using the circuit of Figure 5. An alternate method would be to use the $\overline{CLR}$ control to set the DAC to 0V. Zero calibration should be made before gain calibration.

Gain Adjustment

To adjust the gain of the DAC725, set the DAC to $7FFF_H$ for both DACs. Adjust the gain of each DAC to obtain the full scale voltage of +9.99969V as shown in Table II.

DIGITAL INPUT CODE	BIPOLAR OUTPUT, ±10V			UNITS
	16 Bits	15 Bits	14 Bits	
One LSB	305	610	1224	µV
$7FFF_H$	+9.99969	+9.99939	+9.99878	V
8000_H	–10	–10	–10	V

TABLE II. Digital Input Codes.

INTERFACE LOGIC AND TIMING

The control logic functions are chip select ($\overline{CS}_A$ or $\overline{CS}_B$), write ($\overline{WR}_A$ or $\overline{WR}_B$), latch enable ($\overline{A_0}$, $\overline{A_1}$, $\overline{A_2}$), and clear ($\overline{CLR}$). These pins provide the control functions for the microprocessor interface. There is a write and a chip select for both DAC_A and for DAC_B channels. This allows the 8-bit data word to be latched from the data bus to the input latch or from the input latch to the DAC latch, of DAC_A, DAC_B, or both.

$\overline{A_0}$	$\overline{A_1}$	$\overline{A_2}$	$\overline{WR}$ (A)	$\overline{CS}$ (A)	DESCRIPTION
1	1	0	0	0	DAC latch enabled, Channel A
1	0	1	0	0	Input latch high byte enabled, Channel A
1	0	0	0	0	High byte flows through to DAC, Channel A
0	1	1	0	0	Low byte latched from data bus, Channel A
0	1	0	0	0	Low byte flows through to DAC, Channel A
0	0	1	1	1	Serial input mode for byte latches
X	X	X	1	0	No data is latched
X	X	X	0	1	No data is latched
"1" or "0" indicates TTL Logic Level Channel A shown.					

TABLE III. Truth Table of Data Transfers.

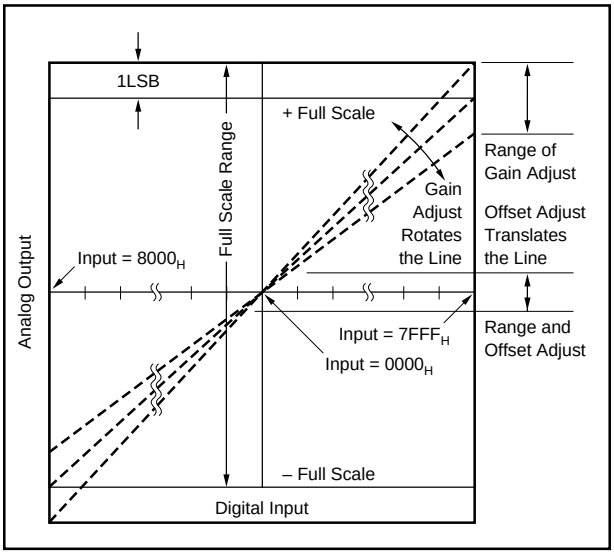


FIGURE 4. Relationship of Zero and Gain Adjustments for the DAC725.

The latch enable lines control which latch is being loaded. Line $\overline{A_1}$ in combination with $\overline{WR}$ and $\overline{CS}$ enables the high byte of the DAC channel to be latched through the byte latch. The $\overline{A_0}$ line, in conjunction with the $\overline{WR}$ and $\overline{CS}$, latches the data for the low byte. When $\overline{A_2}$, $\overline{CS}$, and $\overline{WR}$ are low at the same time, the data is latched through the D/A latch and the DAC changes output voltage. Each latch may be made transparent by maintaining its enable signal at logic "0".

The serial data mode is activated when both $\overline{A_0}$ and $\overline{A_1}$ are at logic low simultaneously. The data (MSB first) is clocked in to pin 13 with clock pulses on the $\overline{WR}$ pin. The data is then latched through to the DAC as a complete 16-bit word selected by $\overline{A_2}$.

The $\overline{CLR}$ line resets both input latches to all zeros and sets the DAC latch to 0000_H. This is the binary code that gives a null, or zero, at the output of the DAC.

The maximum clock rate of the latches is 10MHz. The minimum time between the write ($\overline{WR}$) pulses for successive enables is 20ns. In the serial input mode, the maximum rate at which data can be clocked into the input shift register is 10MHz. The timing of the control signals is given in Figure 6.

INTERVAL	DESCRIPTION	OVER TEMP. ns, min	OVER TEMP. ns, max
t_{DW}	Data valid to end of $\overline{WR}$	80	
t_{CW}	$\overline{CS}$ valid to end of $\overline{WR}$	80	
t_{AW}	$\overline{A_0}$, $\overline{A_1}$, $\overline{A_2}$ valid to end of $\overline{WR}$	80	
t_{WP}	Write pulse width	80	
t_{DH}	Data hold after end of $\overline{WR}$	0	

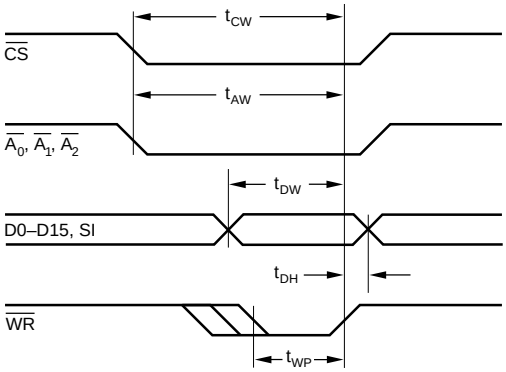


FIGURE 6. Logic Timing Diagram.

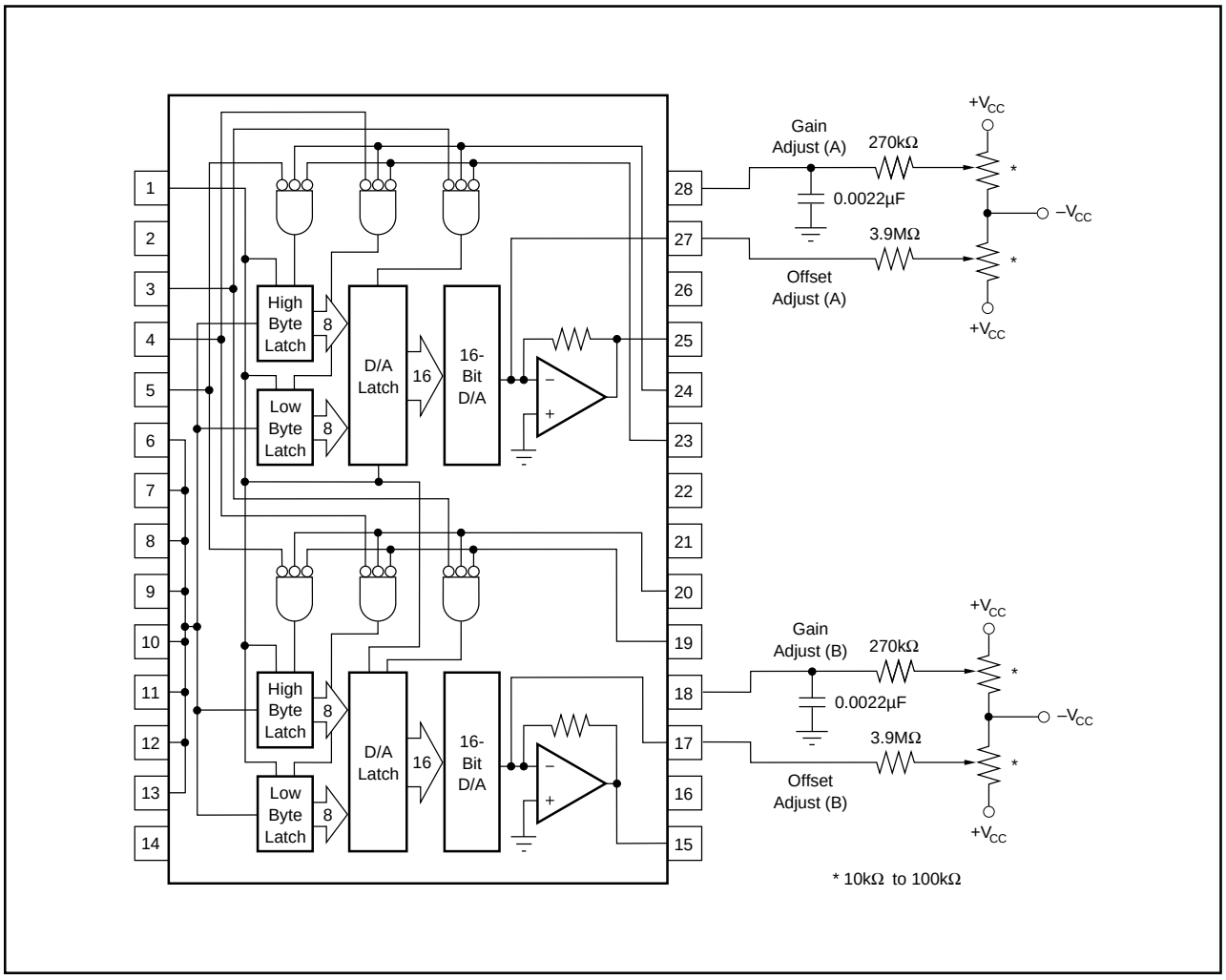


FIGURE 5. Connections for Gain and Offset Adjust.

INSTALLATION

Because of the extremely high accuracy of the D/A converter, system design problems such as grounding and contact resistance become very important. For a 16-bit converter with a +10V full-scale range, 1LSB is 153μV. With a load current of 5mA, series wiring and connector resistance of only 30mΩ will cause the output to be in error by 1LSB. To understand what this means in terms of a system layout, the resistance of typical 1oz copper-clad printed circuit board material is approximately 1/2mΩ per square mil. In the example above, a 10mil-wide conductor 60mil long would cause a 1LSB error in R_2 and R_3 of Figure 7.

In Figure 7, lead and contact resistances are represented as R_2 through R_6. As long as the load resistance (R_L) remains constant, the resistances of R_2 and R_3 will appear as gain errors when the output is sensed across the load. If the output is sensed at the DAC725 output terminal and the system analog common, R_2 and R_3 appear in series with R_L. R_4 has a current through it that varies by only 1% of the nominal 2mA current for all code combinations. This IR drop causes an offset error, and is calibrated out as an offset error.

The current through the digital common varies directly with the digital code that is loaded into the DAC. The current is not the same for each code. If this IR drop is allowed to modulate the analog common, there may be code-dependent errors in the analog output.

The IR drop across R_6 may cause accuracy problems if the analog commons of several circuits are "daisy chained" along the power supply analog common. All analog sense lines should be referenced to the system analog common.

APPLICATIONS

WAVEFORM GENERATION

The DAC725 has attributes that make it ideal for very low distortion waveform synthesis. Due to special design techniques, the feedthrough energy is much lower than that found in other D/A converters available today. In addition to the low feedthrough glitch energy, the input logic will operate with data rates of 10MHz. This makes the DAC725 ideal for waveform synthesis.

PROGRAMMABLE POWER SUPPLIES

The DAC725 is an excellent choice for programmable power supply applications. The DAC outputs may be programmed to track or oppose each other. If the load is floating, and can be driven differentially, the dynamic range will be 17 bits, because the full-scale range doubles for the same sized LSB. The clear line ($\overline{CLR}$) sets both DAC outputs to zero, and would be used at power-up to bring the system up in a safe state. The $\overline{CLR}$ line could also be used if an over-power state is sensed.

ISOLATION

The DAC725 can accept serial input data, which means that only six optoisolators are needed for two DACs. The data is clocked into the input latch using the $\overline{WR}$ pin. The 16-bit data word is latched into the DAC selected by $\overline{A_2}$. When $\overline{A_0}$ and $\overline{A_1}$ are simultaneously low, the serial mode is enabled.

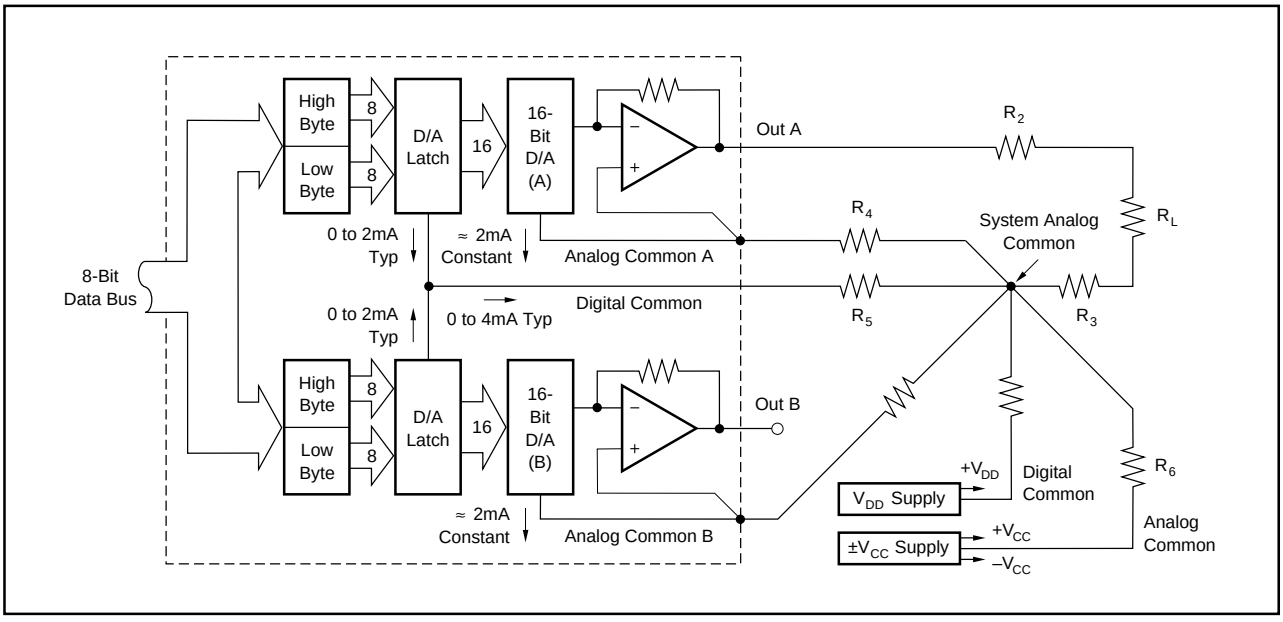


FIGURE 7. System Wiring Example.

PACKAGING INFORMATION

ORDERABLE DEVICE	STATUS(1)	PACKAGE TYPE	PACKAGE DRAWING	PINS	PACKAGE QTY
DAC725JP	NRND	PDIP	NTD	28	13
DAC725KP	NRND	PDIP	NTD	28	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

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